

FIG. 1

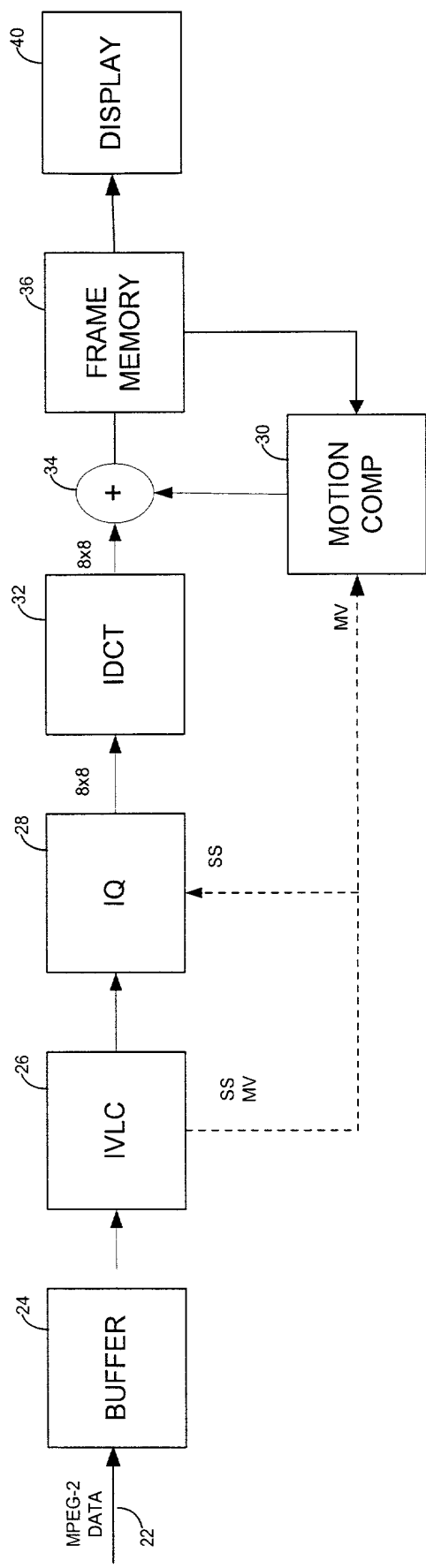


FIG. 2

FIG. 3 is a block diagram of a video decoding system. The system includes a BUFFER (24) that receives MPEG-2 DATA (22). The output of the BUFFER (24) is fed into an IVLC (26) block. The IVLC (26) block outputs an 8x8 signal to an IQ (28) block. The IQ (28) block outputs a 4x8 signal to an IDCT (50) block. The IDCT (50) block outputs a 4x8 signal to an adder (+) (34). The adder (+) (34) also receives a signal from a MOTION COMP (60) block. The output of the adder (+) (34) is fed into a DISPLAY BUFFER (62). The DISPLAY BUFFER (62) is divided into a DISPLAY BUFFER (62) and a REF BUFFER (64). The output of the DISPLAY BUFFER (62) is fed into a SCALER (66). The SCALER (66) outputs a signal to a DISPLAY (68). The MOTION COMP (60) block receives a signal from the REF BUFFER (64) and outputs a signal to the adder (+) (34). The MOTION COMP (60) block also receives a signal from the IVLC (26) block via a dashed line labeled SS and MV.

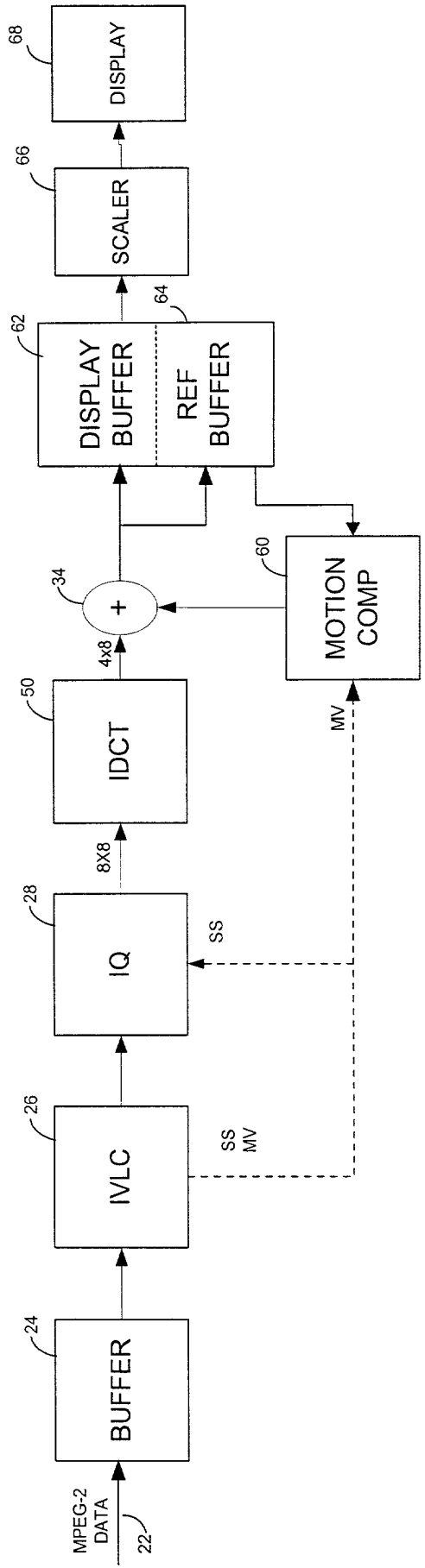


FIG. 3

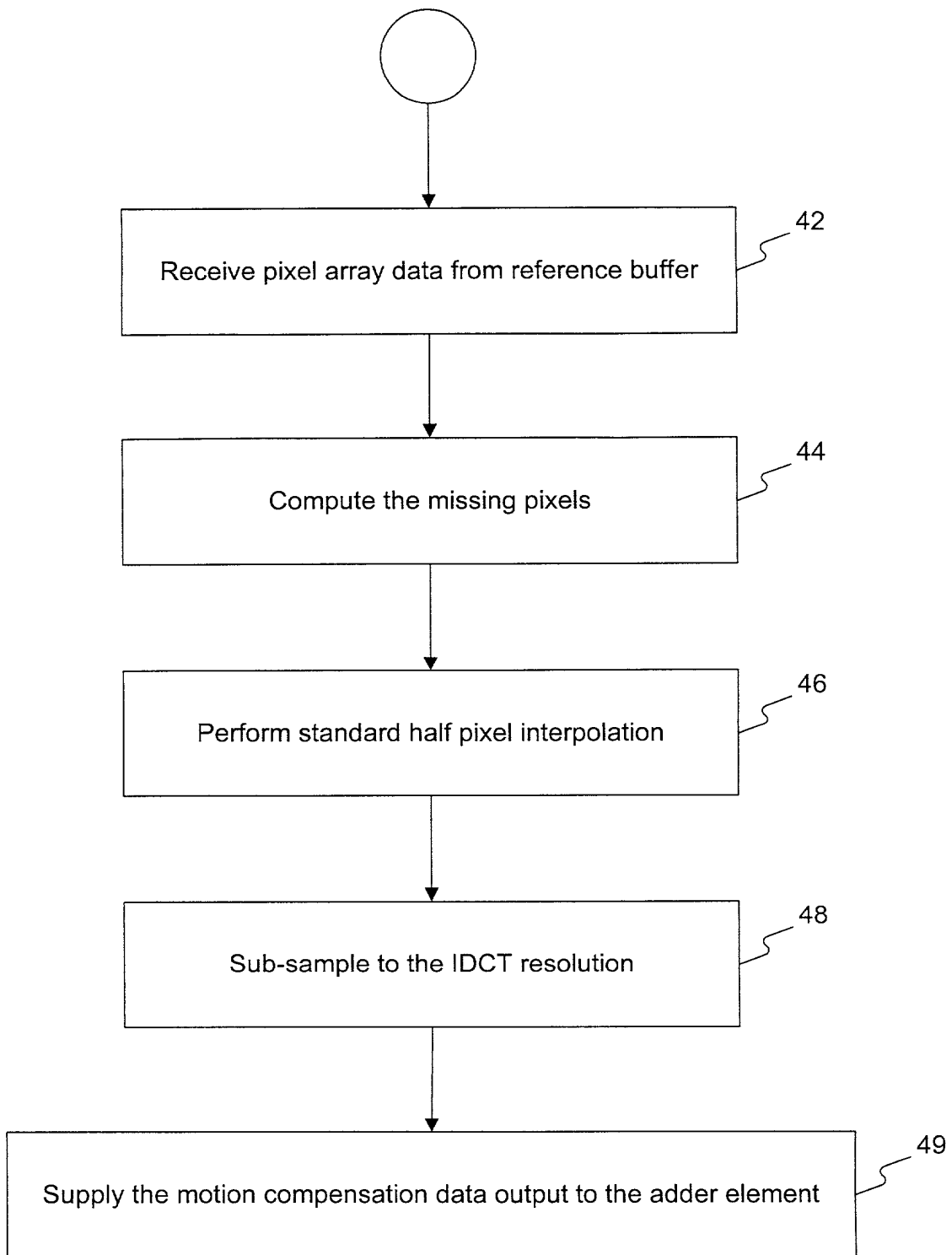


FIG. 4

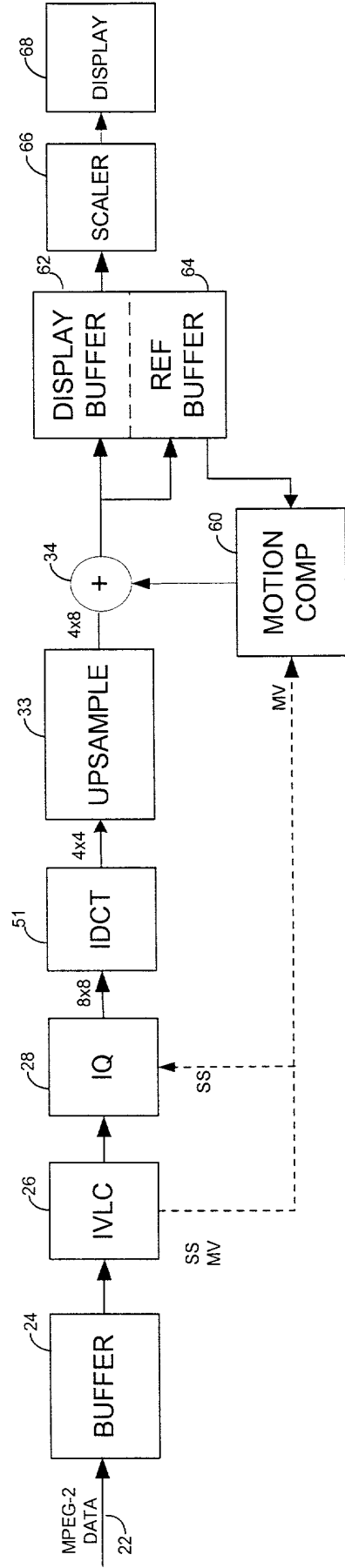


FIG. 5

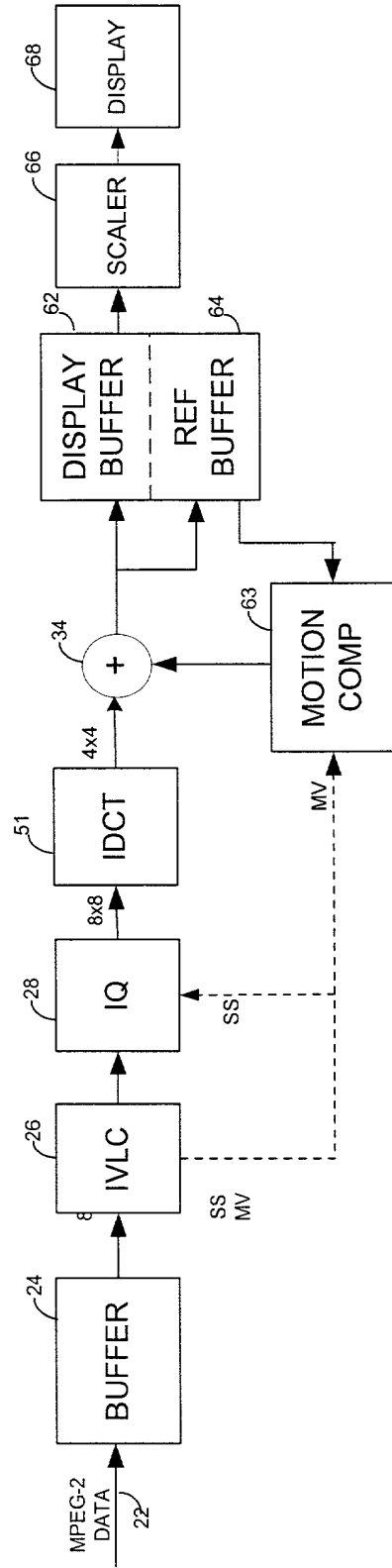


FIG. 6

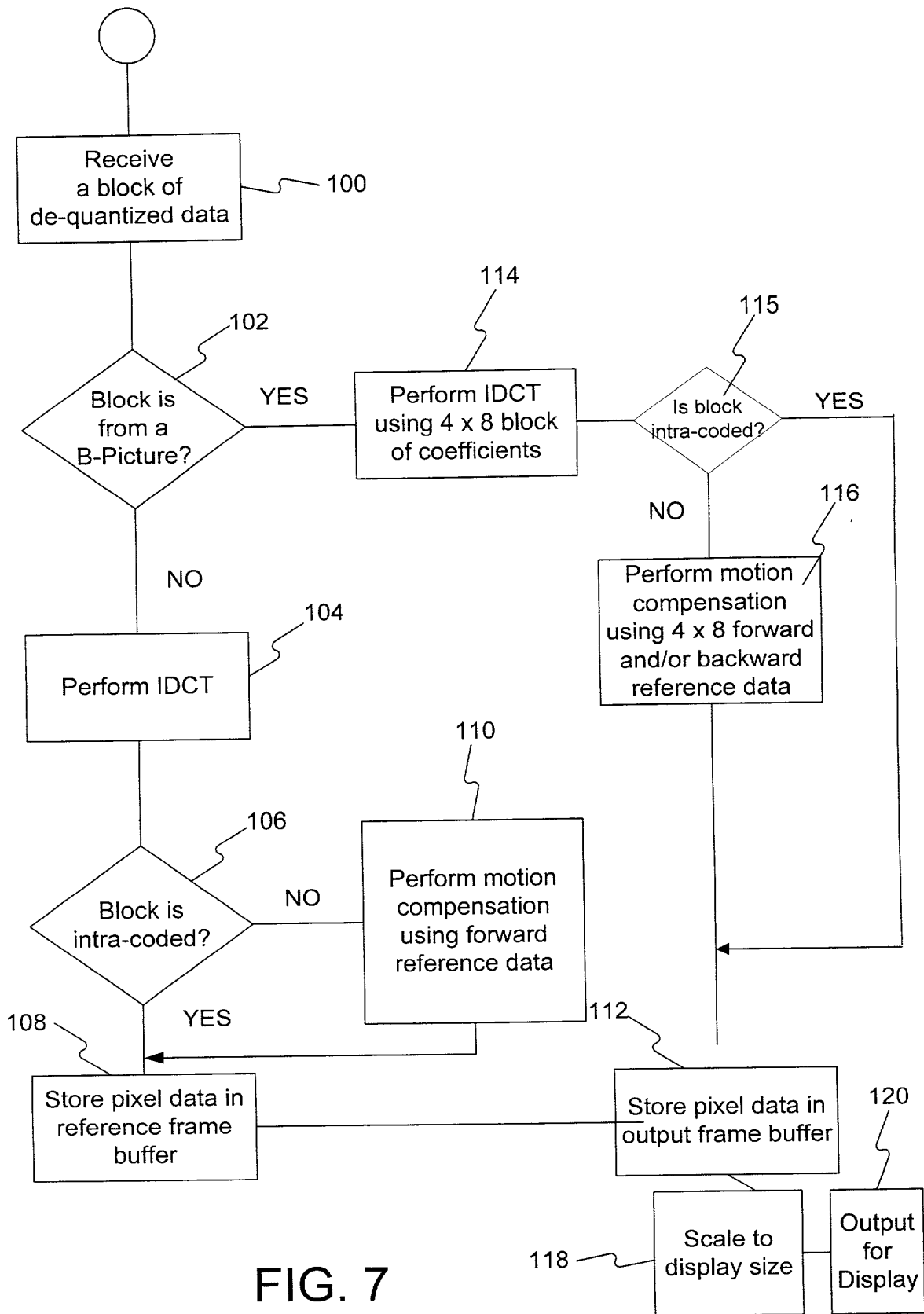


FIG. 7

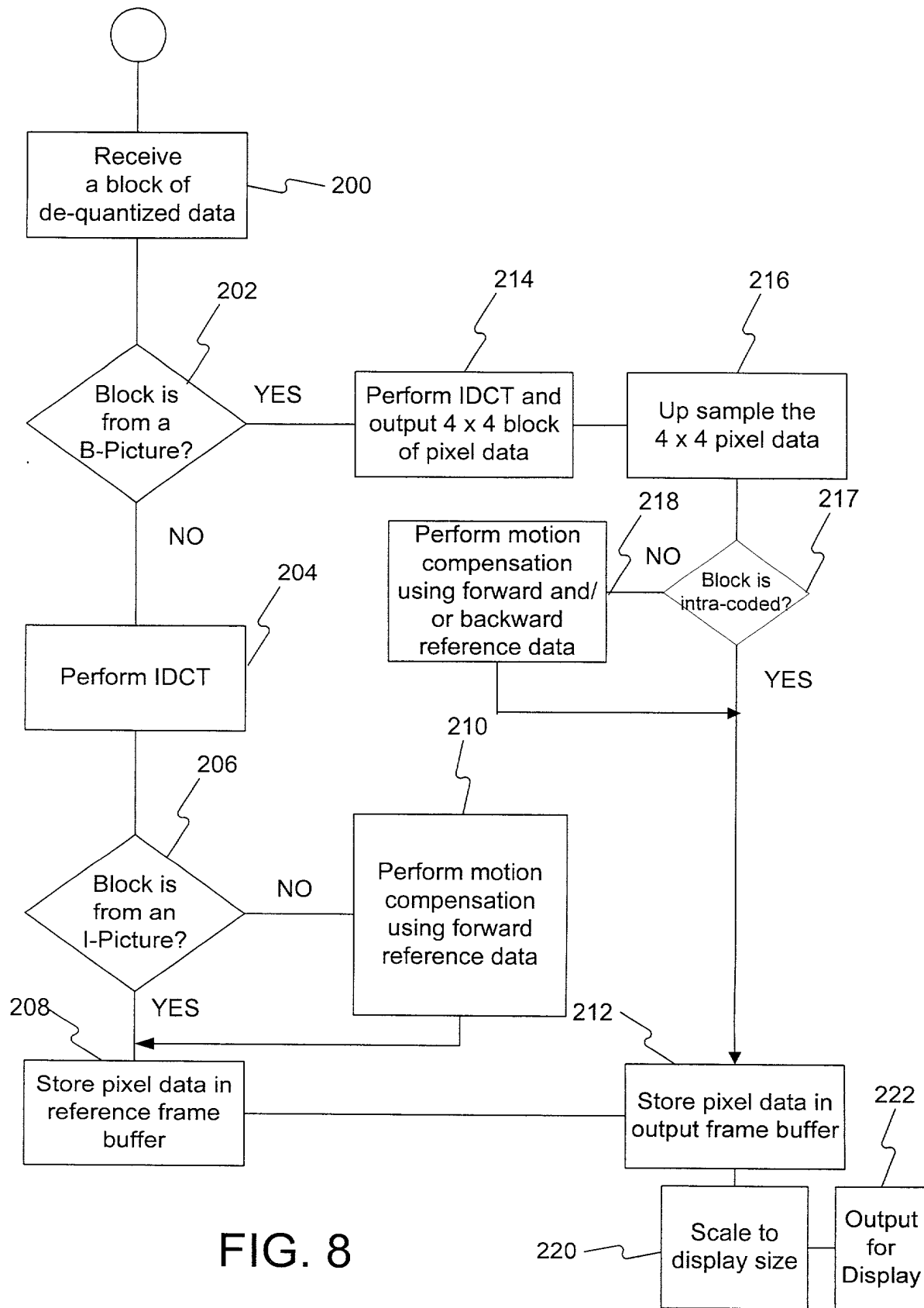


FIG. 8



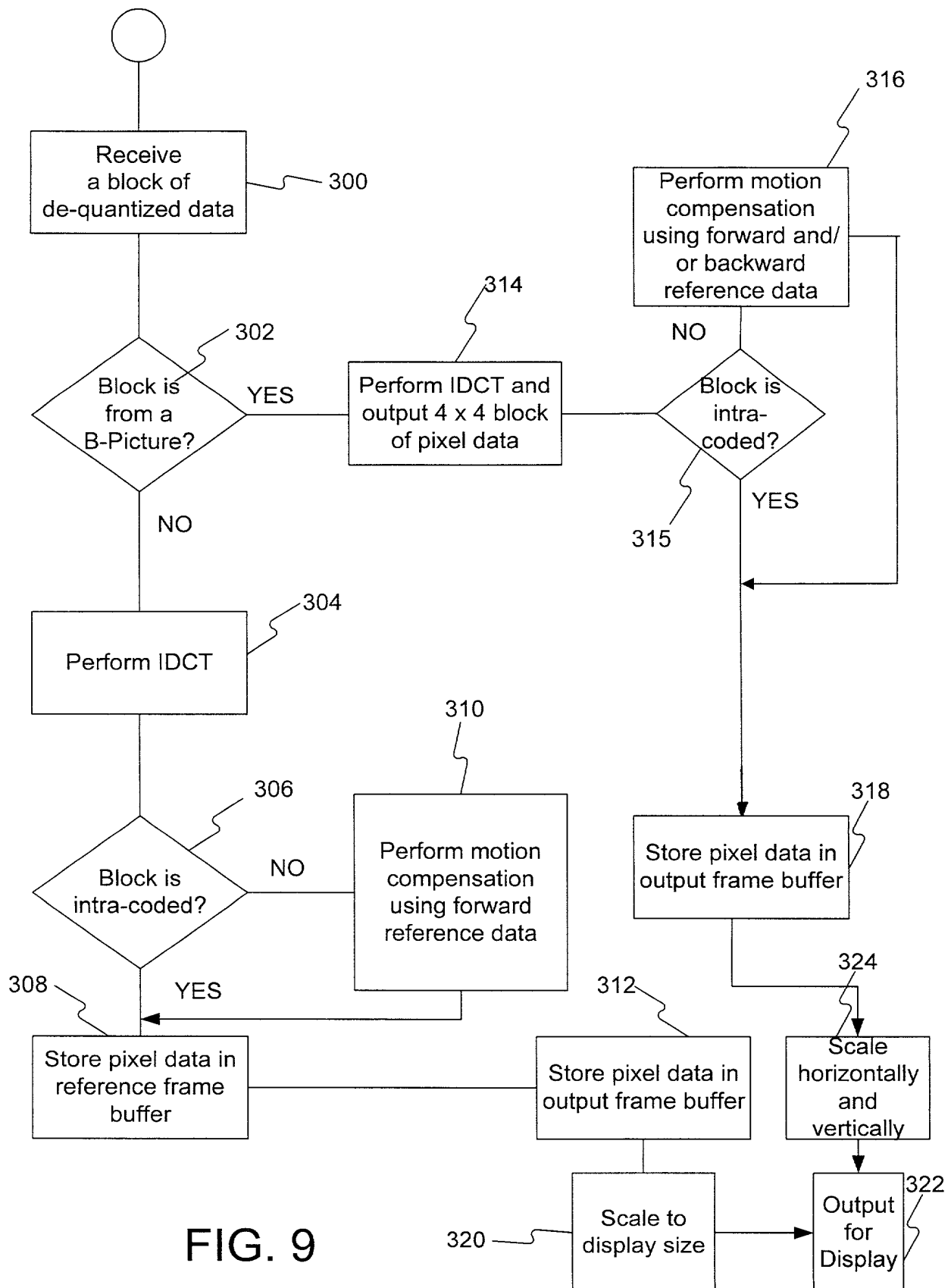
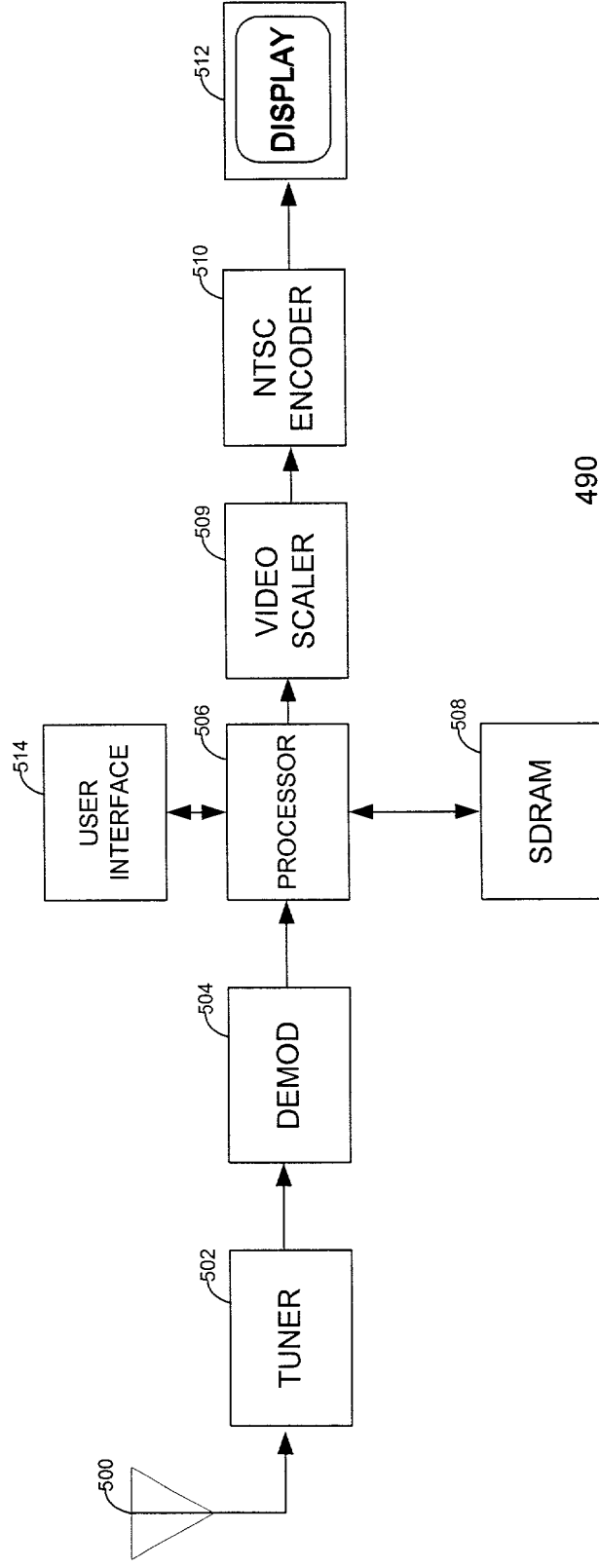


FIG. 9



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FIG. 10